AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A flash memory cell comprising:

a substrate comprising a source and a drain;

a silicon dioxide layer adjoining said substrate;

a dielectric layer adjoining said silicon dioxide layer, said dielectric layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide, wherein said dielectric material comprises a metal oxide;

a polysilicon floating gate adjoining said dielectric layer;

an oxide-nitride-oxide (ONO) layer adjoining said floating gate; and

a control gate adjoining said ONO layer, wherein said substrate, said silicon dioxide layer, said dielectric layer, said floating gate, said ONO layer and said control gate are arranged in a laminate structure, wherein said silicon dioxide layer is sandwiched between said substrate and said dielectric layer, wherein said dielectric layer is sandwiched between said silicon dioxide layer and said floating gate, and wherein said ONO layer is sandwiched between said floating gate and said control gate.

2-7. (Canceled).

8. (Previously Presented) The flash memory cell of Claim 1 wherein said dielectric layer comprises a composite of said metal oxide and a material selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate.

9. (Canceled).

10. (Previously Presented) A flash memory array comprising memory cells, wherein a memory cell comprises:

a substrate comprising a source and a drain;

a tunnel oxide layer adjoining said substrate, said tunnel oxide layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide, wherein said dielectric material comprises a metal oxide;

a first layer comprising a silicon material;

a polysilicon floating gate adjoining said first layer;

an oxide-nitride-oxide (ONO) layer adjoining said floating gate; and

a control gate adjoining said ONO layer, wherein said substrate, said tunnel oxide layer, said first layer, said floating gate, said ONO layer and said control gate are arranged in a laminate structure, wherein said tunnel oxide layer is sandwiched between said substrate and said first layer, wherein said first layer is sandwiched between said tunnel oxide layer and said floating gate, and wherein said ONO layer is sandwiched between said floating gate and said control gate.

11. (Canceled).

12. (Previously Presented) The flash memory array of Claim 10 wherein said silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate.

13-25. (Canceled).